What is claimed is:

1. A MOS transistor comprising:

a gate electrode on a substrate, the gate electrode having a first lateral protrusion extending from a lower portion of a first sidewall of the gate electrode and a second lateral protrusion extending from a lower portion of a second sidewall of the gate electrode;

a drain region in the substrate comprising a first lightly-doped drain region under the first lateral protrusion, a second lightly-doped drain region that is deeper than the first lightly-doped drain region adjacent the first lightly-doped drain region, and a heavily-doped drain region adjacent to the second lightly-doped drain region; and

a source region in the substrate comprising a first lightly-doped source region under the second lateral protrusion, a second lightly-doped source region that is deeper than the first lightly-doped source region adjacent the first lightly-doped source region, and a heavily-doped source region adjacent to the second lightly-doped source region.

2. The MOS transistor of Claim 1, further comprising an insulating gate spacer covering the first and second sidewalls of the gate electrode, wherein the second lightly-doped drain region and the second lightly-doped source region are under bottom portions of the insulating gate spacer.

3. The MOS transistor of Claim 2, wherein the heavily doped drain region is adjacent a first outer sidewall of the insulating gate spacer and wherein the heavily doped source region is adjacent a second outer sidewall of the insulating gate spacer.

4. The MOS transistor of Claim 1, wherein the gate electrode has an inverted T-shape.

5. The MOS transistor of Claim 1, further comprising a gate dielectric layer interposed between the gate electrode and the substrate.

6. The MOS transistor of Claim 2, further comprising a curing thermal oxide layer on the sidewalls of the gate electrode, the second lightly-doped drain region and the second lightly-doped source region.

7. The MOS transistor of Claim 6, wherein the insulating gate spacer is on the curing thermal oxide layer.

8. The MOS transistor of Claim 7, further comprising a spacer etch stop layer interposed between the insulating gate spacer and the curing thermal oxide layer.

9. The MOS transistor of Claim 1, wherein the sidewalls of the first and second lateral protrusions are vertically profiled.

10. The MOS transistor of Claim 1, wherein the sidewalls of the first and second lateral protrusions are sloped at positive angles.

11. The MOS transistor of claim 1 wherein the sidewalls of the first and second lateral protrusions are sloped at negative angles.

12. The MOS transistor of claim 1 further comprising a metal silicide layer on the upper surface of the gate electrode, the surface of the heavily-doped drain region and the surface of the heavily-doped source region.

13. A CMOS integrated circuit device comprising:

a semiconductor substrate having an NMOS transistor region and a PMOS transistor region therein;

an inverted T-shaped NMOS gate electrode on the NMOS transistor region;

an inverted T-shaped PMOS gate electrode on the PMOS transistor region;

first gate spacers on the sidewalls of the NMOS gate electrode;

second gate spacers on the sidewalls of the PMOS gate electrode;

a pair of first n-type lightly-doped regions in the substrate under portions of the NMOS gate electrode;

a pair of second n-type lightly-doped regions in the substrate, each of which is under a portion of the first gate spacers, the second n-type lightly-doped regions being deeper than the first n-type lightly-doped regions;

a pair of n-type heavily-doped regions in the substrate, each of which is adjacent to one of the second n-type lightly-doped regions; and

a pair of p-type heavily-doped regions in the substrate adjacent the PMOS gate electrode.

14. The CMOS integrated circuit device of Claim 13, wherein the NMOS gate electrode and the PMOS gate electrode are the same height above the substrate.

15. The CMOS integrated circuit device of Claim 13, further comprising a gate dielectric layer interposed between the NMOS gate electrode and the substrate and between the PMOS gate electrode and the substrate.

16. The CMOS integrated circuit device of Claim 15, wherein the depth of each of the second n-type lightly-doped regions is about the same as the combined depth of one of the first n-type lightly-doped regions, the gate dielectric layer and the crossbar portion of the NMOS gate electrode.

17. The CMOS integrated circuit device of Claim 13, wherein the sidewalls of the crossbar portion of the inverted T-shaped NMOS gate electrode are vertically profiled and wherein the sidewalls of the crossbar portion of the inverted T-shaped PMOS gate electrode are vertically profiled.

18. The CMOS integrated circuit device of Claim 13, wherein at least one of the sidewalls of the crossbar portion of the inverted T-shaped NMOS gate electrode is sloped at a positive angle and wherein at least one of the sidewalls of the crossbar portion of the inverted T-shaped PMOS gate electrode is sloped at a positive angle.

19. The CMOS integrated circuit device of Claim 13, wherein at least one of the sidewalls of the crossbar portion of the inverted T-shaped NMOS gate electrode is sloped at a negative angle and wherein at least one of the sidewalls of the crossbar portion of the inverted T-shaped PMOS gate electrode is sloped at a negative angle.

20. The CMOS integrated circuit device of Claim 13, further comprising a metal silicide layer on the upper surface of the NMOS gate electrode, the upper surface of the PMOS gate electrode, the n-type heavily-doped regions, and the p-type heavily-doped regions.

21. The CMOS integrated circuit device of Claim 13, further comprising an n-type pocket impurity region covering at least the sidewalls of the p-type heavily-doped regions, the n-type pocket impurity region being extended to the region under the PMOS gate electrode.

22. The CMOS integrated circuit device of Claim 13, further comprising a pair of first p-type lightly-doped regions in the substrate under portions of the PMOS gate electrode and a pair of second p-type lightly-doped regions in the substrate, each of which is under a portion of the second gate spacers, each the second p-type lightly-doped region being deeper than the first p-type lightly-doped regions, shallower than the p-type heavily-doped regions, and interposed between one of the first p-type lightly-doped regions and one of the p-type heavily-doped regions.

23. A method of fabricating a MOS transistor comprising the steps of:

defining an active region in a semiconductor substrate;

forming a gate electrode on the active region, the gate electrode having a first lateral protrusion extending from a lower portion of a first sidewall of the gate electrode and a second lateral protrusion extending from a lower portion of a second sidewall of the gate electrode;

forming a drain region in the substrate comprising a first lightly-doped drain region under the first lateral protrusion, a second lightly-doped drain region that is deeper than the first lightly-doped drain region adjacent the first lightly-doped drain region, and a heavily-doped drain region adjacent to the second lightly-doped drain region; and

forming a source region in the substrate comprising a first lightly-doped source region under the second lateral protrusion, a second lightly-doped source region that is deeper than the first lightly-doped source region adjacent the first lightly-doped source region, and a heavily-doped source region adjacent to the second lightly-doped source region.

24. The method of Claim 23, wherein forming a gate electrode on the active region comprises:

forming a first layer on the surface of the substrate;

forming a second layer on the first layer;

forming a groove that penetrates the second layer and the first layer, wherein the width of the groove in the first layer is greater than the width of the groove in the second layer so as to form a pair of undercut regions in the first layer; and

forming the inverted T-shaped gate pattern in the groove that has first and second lateral protrusions that fill the pair of undercut regions.

25. The method of Claim 24, wherein the bottom of the groove exposes a portion of the active region and further comprising forming a gate dielectric layer on the exposed portion of the active region.

26. The method of Claim 25, further comprising:

removing the second layer and the first layer; and

implanting impurity ions into the active region using the inverted T-shaped gate pattern as an implant mask so as to simultaneously form the first lightly-doped drain region, the first lightly-doped source region, the second lightly-doped drain region and the second lightly-doped source region.

27. The method of Claim 26, further comprising:

forming gate spacers on the sidewalls of the inverted T-shaped gate pattern; and

implanting impurity ions into the active region using the gate pattern and the gate spacers as an implant mask so as to form a heavily-doped drain region in the active region adjacent to one of the outer sidewalls of the gate spacers and a heavily-doped source region in the active region adjacent to the other one of the outer sidewalls of the gate spacers.

28. The method of Claim 27, wherein the first layer is a buffer layer.

29. The method of Claim 28, wherein the second layer comprises a molding layer and wherein forming the groove comprises patterning the molding layer to expose a portion of the buffer layer and then etching the exposed portion of the buffer layer in an isotropic manner so as to form the pair of undercut regions.

30. The method of Claim 29, wherein each of the pair of undercut regions have a vertically profiled outer sidewall.

31. The method of Claim 29, wherein each of the pair of undercut regions have an outer sidewall that is sloped at a positive angle.

32. The method of Claim 29, wherein each of the pair of undercut regions have an outer sidewall that is sloped at a negative angle.

33. The method of Claim 25, wherein forming the inverted T-shaped gate pattern comprises:

forming an undoped semiconductor layer on the substrate provided with the gate dielectric layer thereon to fill the groove; and

planarizing the undoped semiconductor layer until the surface of the second layer is exposed to form the undoped gate pattern in the groove.

34. The method of Claim 25 wherein forming the groove that penetrates the second layer and the first layer comprises:

forming a capping layer on the second layer;

patterning the capping layer to form a trench region that exposes a portion of the second layer;

forming a trench spacer on the sidewalls of the trench region;

etching the second layer using the capping layer and the trench spacer as an etch mask so as to expose a portion of the first layer; and

etching the exposed portion of the first layer in an isotropic manner so as to form the pair of undercut regions.

35. The method of Claim 34, wherein forming the inverted T-shaped gate pattern comprises:

forming an undoped semiconductor layer on the substrate provided with the gate dielectric layer thereon to fill the groove; and

planarizing the undoped semiconductor layer, the capping layer, and the trench spacer until the upper part of the second layer is exposed to form the undoped gate pattern in the groove.

36. The method of Claim 25, wherein forming the groove that penetrates the second layer and the first layer comprises:

forming a capping layer on the second layer;

etching the capping layer and the second layer to form a trench region in the capping layer and in a portion of the trench layer;

forming a spacer dielectric layer on the semiconductor substrate provided with the trench region therein;

etching the spacer dielectric layer to form a trench spacer on the sidewalls of the trench region;

etching the second layer below the trench region to expose a portion of the first layer; and

etching the exposed first layer in the isotropic manner so as to form the pair of undercut regions in the first layer.

37. The method of Claim 36, wherein forming the inverted T-shaped gate pattern comprises:

forming an undoped semiconductor layer on the substrate provided with the gate dielectric layer thereon to fill the groove; and

planarizing the undoped semiconductor layer, the capping layer, and the trench spacer until the upper part of the second layer is exposed to form the undoped gate pattern in the groove.

38. The method of Claim 28, wherein the buffer layer has a thickness of 100-300 angstroms.

39. The method of Claim 28, wherein the buffer layer has a thickness of less than 100 angstroms.

40. The method of Claim 28, wherein the buffer layer has a thickness of 300-500 angstroms.

41. The method of Claim 27, further comprising forming a curing thermal oxide layer on the substrate prior to forming the gate spacers, wherein the curing thermal oxide layer acts as an etch stop layer during the formation of the gate spacers.

42. The method of Claim 41, further comprising forming a spacer etch stop layer on the curing thermal oxide layer, wherein the spacer etch stop layer is formed from a dielectric material having etch selectivity with respect to the gate spacers.

43. The method of Claim 27, further comprising the steps of:

exposing the upper surface of the gate pattern and the upper surfaces of the heavily-doped regions; and

forming a metal silicide layer selectively on the exposed gate pattern and the exposed heavily-doped regions.

44. The method of Claim 28, wherein the buffer layer is formed from silicon oxide and the second layer is formed from silicon nitride.

45. The method of Claim 33 wherein the undoped semiconductor layer comprises an undoped silicon layer.

46. The method of Claim 24, further comprising selectively implanting n-type impurity ions into the first gate pattern and then annealing the first gate pattern prior to removing the second layer and the first layer.

47. The method of Claim 46, wherein the n-type impurity ions are phosphorous ions.

48. The method of Claim 46, wherein the annealing is carried out by rapid thermal process with the temperature range of 900-1200 degrees Centigrade.

49. A method for CMOS transistor comprising the steps of:

providing a semiconductor substrate having an NMOS transistor region and a PMOS transistor region therein;

defining a first active region in the NMOS transistor region and a second active region in the PMOS transistor region;

forming a buffer layer and a molding layer on the semiconductor substrate;

forming a first gate pattern groove that penetrates the molding layer and the buffer layer to expose a portion of the first active region, wherein the first gate pattern groove has a pair of undercut regions in the buffer layer;

forming a second gate pattern groove that penetrates the molding layer and the buffer layer to expose a portion of the second active region, wherein the second gate pattern groove has a pair of undercut regions in the buffer layer;

forming a gate dielectric layer on the exposed first active region and the exposed second active region;

forming a first undoped gate pattern in the first gate pattern groove and a second undoped gate pattern in the second gate pattern groove;

implanting n-type impurity ions into the first undoped gate pattern;

annealing the first undoped gate pattern; and

removing the molding layer.

50. The method of Claim 49 wherein the buffer layer and the molding layer are formed from silicon oxide and silicon nitride, respectively.

51. The method of Claim 49, wherein forming the first undoped gate pattern and the second undoped gate pattern comprises:

forming an undoped silicon layer on the substrate provided with the first gate pattern groove and the second gate pattern groove, the undoped silicon layer filling the first gate pattern groove and the second gate pattern groove; and

planarizing the undoped silicon layer until the upper part of the molding layer is exposed.

52. The method of Claim 49, wherein the molding layer is removed using a wet etchant.

53. The method of Claim 49, further comprising:

forming an n-type source/drain region in the first active region on each side of the first gate pattern; and

forming a p-type source/drain region in the second active region on each side of the second gate pattern.